WHAT IS CLAIMED IS:

1. A level shifter comprising:

an inverter having an input node and an intermediate node, the input node having a logic state, the intermediate node having a logic state opposite of the logic state of the input node;

a first transistor that contacts the inverter and a first output node, the first output node having a logic state;

a second transistor that contacts the inverter and a second output node, the second output node having a logic state opposite the logic state of the first output node;

a third transistor that contacts the first transistor and the first output node; and

a fourth transistor that contacts the second transistor and the second output node.

2. The level shifter of claim 1 and further comprising:

a fifth transistor that contacts the second transistor;

a sixth transistor that contacts the fifth transistor; and

a seventh transistor that contacts the fifth transistor, the sixth transistor, and the first output node.

3. The level shifter of claim 2 wherein the sixth transistor contacts the first output node.

4. The level shifter of claim 3 wherein the inverter contacts a first supply voltage.

5. The level shifter of claim 4 wherein the first, second, fifth, and seventh transistors are connected to ground, and the third, fourth,

and sixth transistors are connected to a second supply voltage, the second supply voltage being greater than the first supply voltage.

6. The level shifter of claim 3 wherein the fifth and sixth transistors are MOS transistors, and the seventh transistor is a bipolar transistor.

7. The level shifter of claim 3 wherein the third transistor has a gate and a drain, and the fourth transistor has a gate that contacts the drain of the third transistor, and a drain that contacts the gate of the third transistor.

8. The level shifter of claim 7 and further comprising:

an eighth transistor that contacts the first transistor;

a ninth transistor that contacts the eighth transistor; and

a tenth transistor that contacts the eighth transistor, the ninth transistor, and the second output node.

9. The level shifter of claim 8 wherein the ninth transistor contacts the second output node.

10. The level shifter of claim 9 wherein the inverter contacts a first supply voltage.

11. The level shifter of claim 10 wherein the first, second, fifth, seventh, eighth, and tenth transistors are connected to ground, and the third, fourth, sixth, and ninth transistors are connected to a second supply voltage, the second supply voltage being greater than the first supply voltage.

12. The level shifter of claim 9 wherein the fifth and sixth transistors are MOS transistors, and the seventh transistor is a bipolar transistor.

13. The level shifter of claim 1 wherein the inverter is connected to a first supply voltage, and the third and fourth transistors are connected to a second supply voltage, the second supply voltage being greater than the first supply voltage.

14. A method of level shifting a voltage, the method comprising the step of pulling down an intermediate voltage on a first intermediate node to a first value when an input voltage on an input node has a logic high, the first value turning off a first transistor and a second transistor, the logic high turning on a third transistor and a fourth transistor, the third transistor pulling down an output voltage on an output node, the fourth transistor pulling down an intermediate voltage on a second intermediate node to a second value, the second value turning on a fifth transistor that pulls down the output voltage on the output node.